

## N-Channel Depletion-Mode Vertical DMOS FET

### Features

- High Input Impedance
- Low Input Capacitance
- Fast Switching Speeds
- Low On-resistance
- Free from Secondary Breakdown
- Low Input and Output Leakage

### Applications

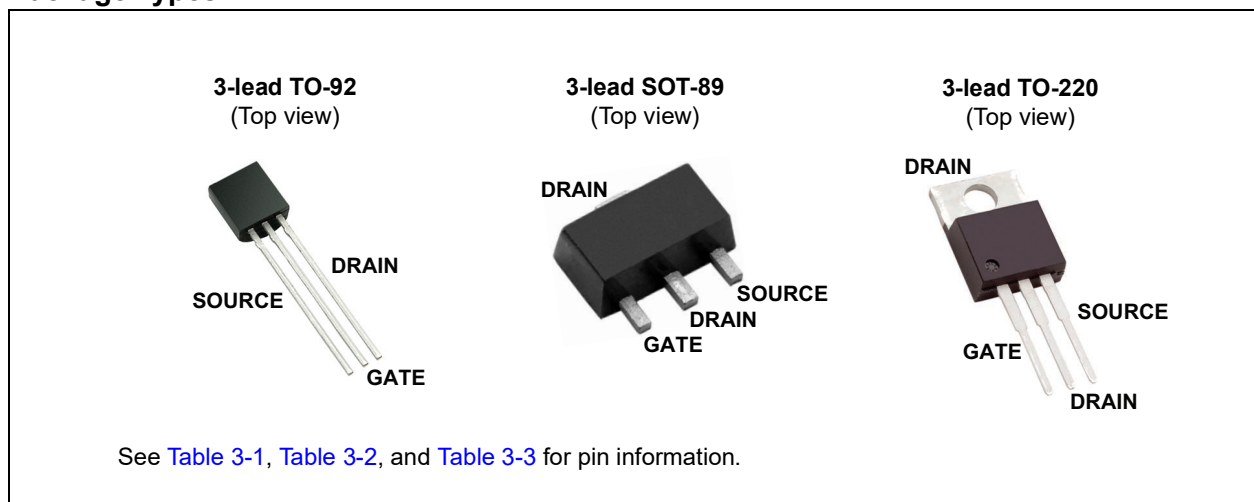
- Normally-on Switches
- Solid-state Relays
- Converters
- Linear Amplifiers
- Constant-current Sources
- Power Supply Circuits
- Telecommunication Switches

### Description

The DN2540 is a low-threshold Depletion-mode (normally-on) transistor that uses an advanced vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power-handling capabilities of bipolar transistors and the high-input impedance and positive-temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Types



# DN2540

## 1.0 ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS†

Drain-to-Source Voltage.....	$BV_{DSX}$
Drain-to-Gate Voltage.....	$BV_{DGX}$
Gate-to-Source Voltage.....	$\pm 20V$
Operating Ambient Temperature, $T_A$ .....	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, $T_S$ .....	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = 25^{\circ}C$  unless otherwise specified. All DC parameters are 100% tested at  $25^{\circ}C$  unless otherwise stated. Pulse test: 300  $\mu s$  pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	$BV_{DSX}$	400	—	—	V	$V_{GS} = -5V, I_D = 100 \mu A$
Gate-to-Source Off Voltage	$V_{GS(OFF)}$	-1.5	—	-3.5	V	$V_{DS} = 25V, I_D = 10 \mu A$
Change in $V_{GS(OFF)}$ with Temperature	$\Delta V_{GS(OFF)}$	—	—	-4.5	mV/ $^{\circ}C$	$V_{DS} = 25V, I_D = 10 \mu A$ ( <b>Note 1</b> )
Gate Body Leakage Current	$I_{GSS}$	—	—	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Drain-to-Source Leakage Current	$I_{D(OFF)}$	—	—	10	$\mu A$	$V_{DS} = \text{Maximum rating}, V_{GS} = -10V$
		—	—	1	mA	$V_{DS} = 0.8 \text{ Maximum rating}, V_{GS} = -10V, T_A = 125^{\circ}C$ ( <b>Note 1</b> )
Saturated Drain-to-Source Current	$I_{DSS}$	150	—	—	mA	$V_{GS} = 0V, V_{DS} = 25V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	17	25	$\Omega$	$V_{GS} = 0V, I_D = 120 \text{ mA}$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1.1	%/ $^{\circ}C$	$V_{GS} = 0V, I_D = 120 \text{ mA}$ ( <b>Note 1</b> )

**Note 1:** Specification is obtained by characterization and is not 100% tested.

## AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = 25^\circ\text{C}$  unless otherwise specified. Specification is obtained by characterization and is not 100% sample tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	$G_{FS}$	—	325	—	mmho	$V_{DS} = 10\text{V}, I_D = 100\text{ mA}$
Input Capacitance	$C_{ISS}$	—	200	300	pF	$V_{GS} = -10\text{V},$ $V_{DS} = 25\text{V},$ $f = 1\text{ MHz}$
Common-Source Output Capacitance	$C_{OSS}$	—	12	30	pF	
Reverse Transfer Capacitance	$C_{RSS}$	—	1	5	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	—	10	ns	$V_{DD} = 25\text{V},$ $I_D = 150\text{ mA},$ $R_{GEN} = 25\Omega,$
Rise Time	$t_r$	—	—	15	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	—	15	ns	
Fall Time	$t_f$	—	—	20	ns	
<b>DIODE PARAMETER</b>						
Diode Forward Voltage Drop	$V_{SD}$	—	—	1.8	V	$V_{GS} = -10\text{V}, I_{SD} = 120\text{ mA}$ ( <b>Note 1</b> )
Reverse Recovery Time	$t_{rr}$	—	800	—	ns	$V_{GS} = -10\text{V}, I_{SD} = 1\text{ A}$

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested at  $25^\circ\text{C}$ . Pulse test: 300  $\mu\text{s}$  pulse, 2% duty cycle

## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Ambient Temperature	$T_A$	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	$T_S$	-55	—	+150	$^\circ\text{C}$	
<b>PACKAGE THERMAL RESISTANCE</b>						
3-lead TO-92	$\theta_{JA}$	—	132	—	$^\circ\text{C/W}$	
3-lead SOT-89	$\theta_{JA}$	—	133	—	$^\circ\text{C/W}$	
3-lead TO-220	$\theta_{JA}$	—	29	—	$^\circ\text{C/W}$	

## THERMAL CHARACTERISTICS

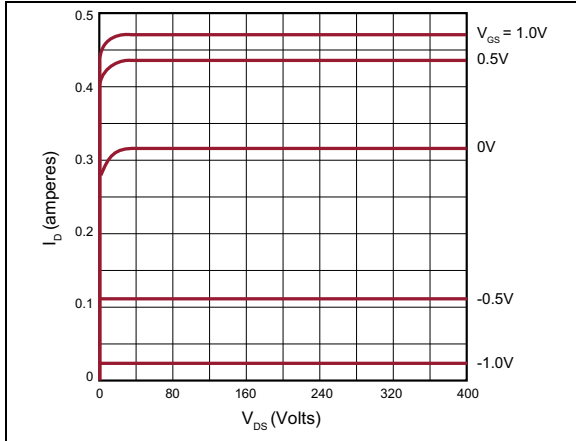
Package	$I_D$ (Note 1) (Continuous) (mA)	$I_D$ (Pulsed) (mA)	Power Dissipation at $T_A = 25^\circ\text{C}$ (Note 2) (W)	$I_{DR}$ (Note 1) (mA)	$I_{DRM}$ (mA)
3-lead TO-92	120	500	1	120	500
3-lead SOT-89	170	500	1.6	170	500
3-lead TO-220	500	500	15	500	500

**Note 1:**  $I_D$  (continuous) is limited by maximum  $T_J$ .

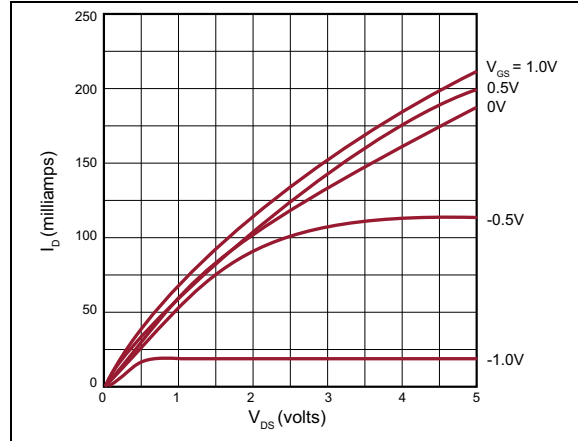
**2:** Mounted on an FR4 board, 25 mm x 25 mm x 1.57 mm

## 2.0 TYPICAL PERFORMANCE CURVES

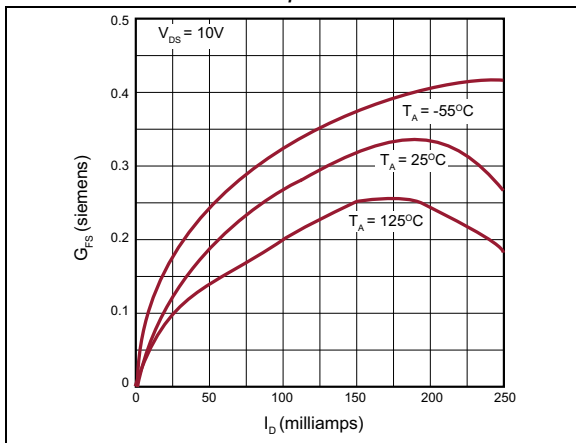
**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.



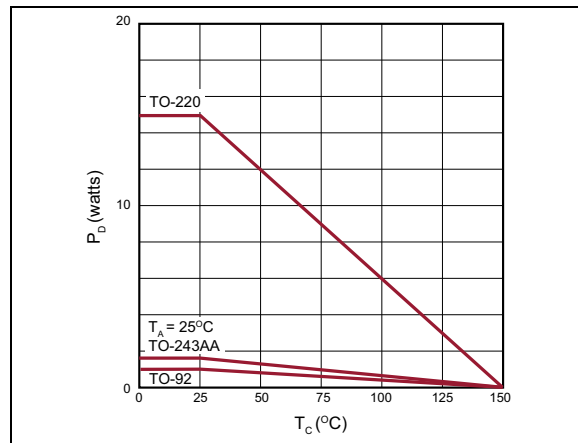
**FIGURE 2-1:** Output Characteristics.



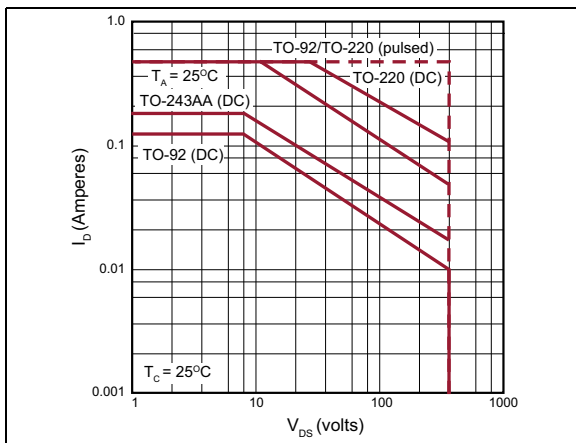
**FIGURE 2-4:** Saturation Characteristics.



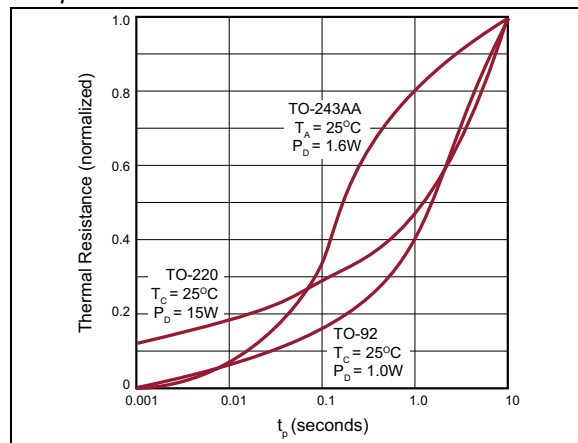
**FIGURE 2-2:** Transconductance vs. Drain Current.



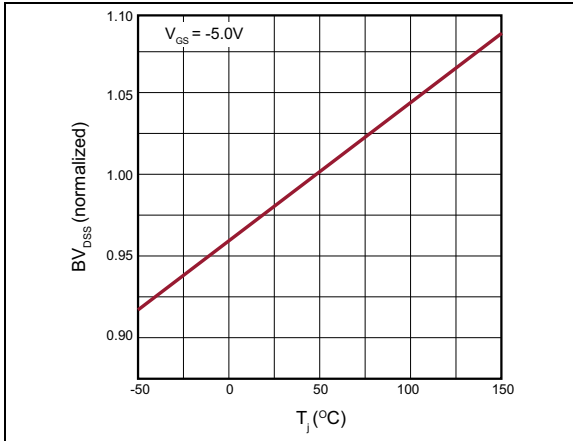
**FIGURE 2-5:** Power Dissipation vs. Case Temperature.



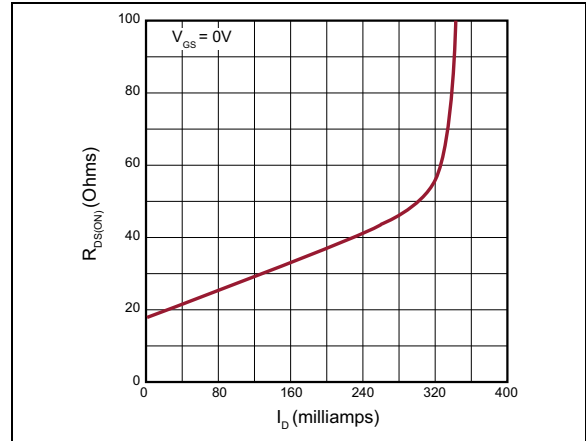
**FIGURE 2-3:** Maximum Rated Safe Operating Area.



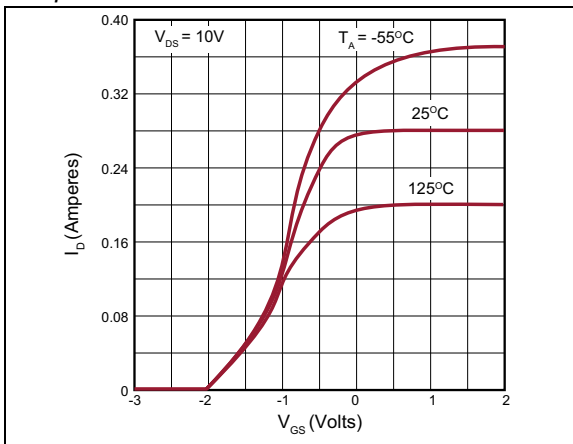
**FIGURE 2-6:** Thermal Response Characteristics.



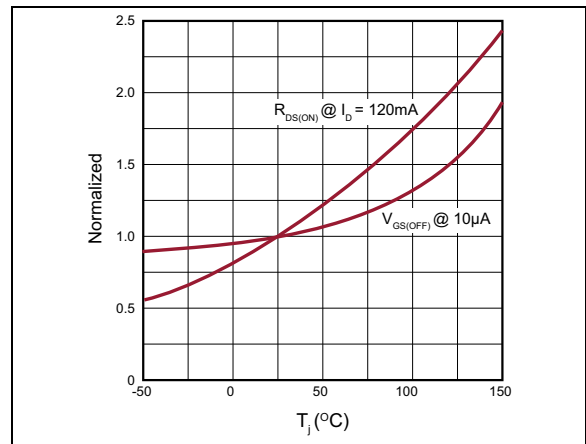
**FIGURE 2-7:**  $BV_{DSV}$  Variation with Temperature.



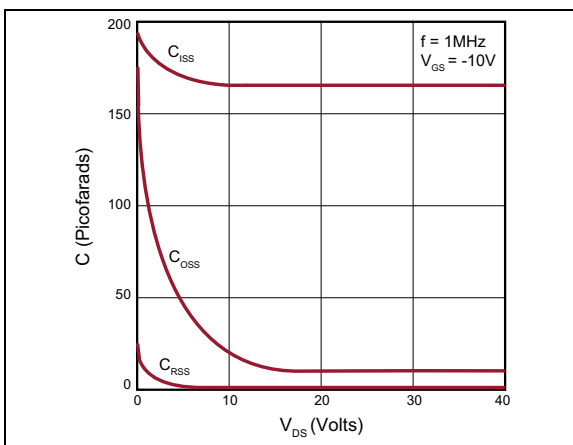
**FIGURE 2-10:** On-Resistance vs. Drain Current.



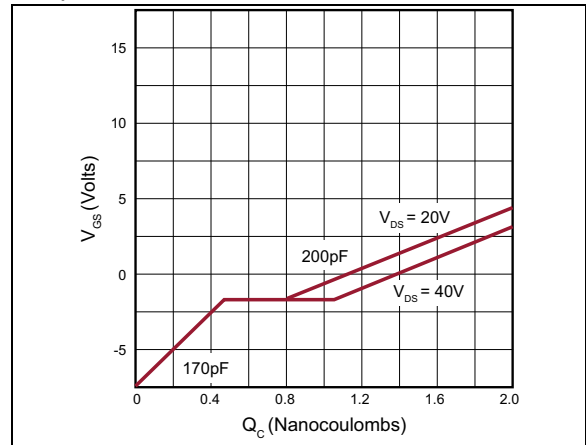
**FIGURE 2-8:** Transfer Characteristics.



**FIGURE 2-11:**  $V_{GS(OFF)}$  and  $R_{DS(ON)}$  with Temperature.



**FIGURE 2-9:** Capacitance vs. Drain-to-Source Voltage.



**FIGURE 2-12:** Gate Drive Dynamic Characteristics.

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## 3.0 PIN DESCRIPTION

Table 3-1, Table 3-2, and Table 3-3 show the description of pins in DN2540. Refer to **Package Types** for the location of pins.

**TABLE 3-1: 3-LEAD TO-92 PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	Source	Source
2	Gate	Gate
3	Drain	Drain

**TABLE 3-2: 3-LEAD SOT-89 PIN FUNCTION TABLE**

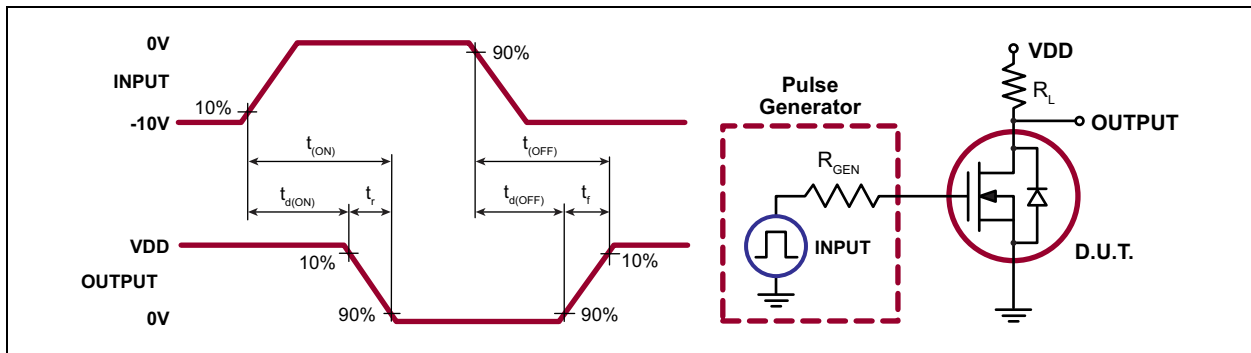
Pin Number	Pin Name	Description
1	Gate	Gate
2	Drain	Drain
3	Source	Source
4	Drain	Drain

**TABLE 3-3: 3-LEAD TO-220 FUNCTION TABLE**

Pin Number	Pin Name	Description
1	Gate	Gate
2	Drain	Drain
3	Source	Source
4	Drain	Drain

## 4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 shows the switching waveforms and test circuit for DN2540.



**FIGURE 4-1:** Switching Waveforms and Test Circuit.

**TABLE 4-1: PRODUCT SUMMARY**

$BV_{DSX}/BV_{DGX}$ (V)	$R_{DS(ON)}$ (Maximum) ( $\Omega$ )	$I_{DSS}$ (Minimum) (mA)
400	25	150

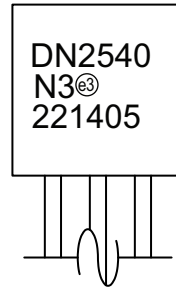
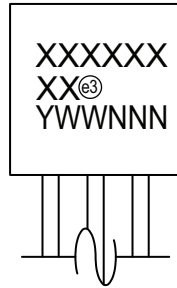
# DN2540

## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

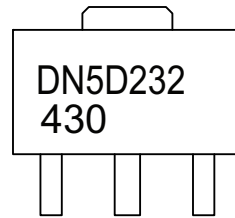
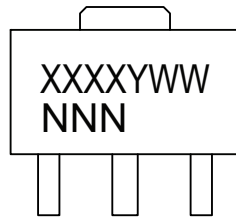
3-lead TO-92

Example



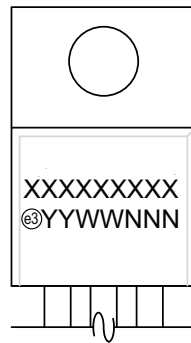
3-lead SOT-89

Example



3-lead TO-220

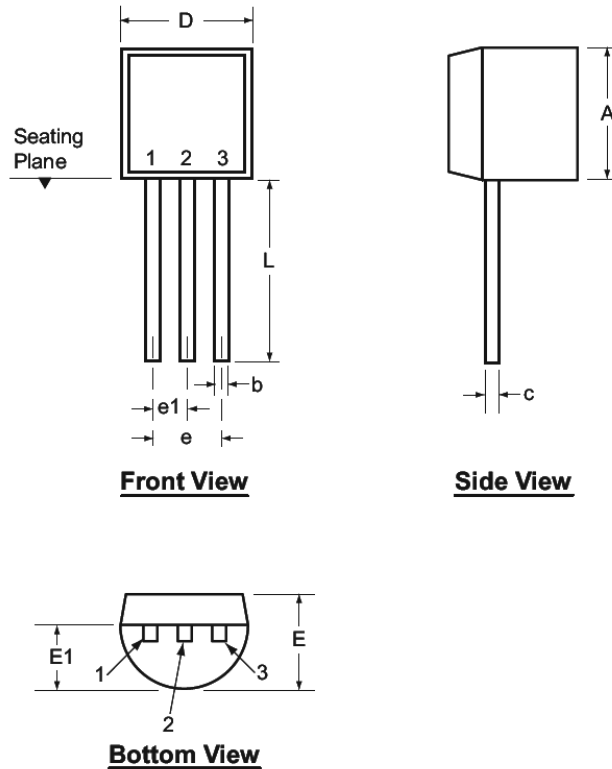
Example



<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

## 3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

Symbol	A	b	c	D	E	E1	e	e1	L	
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

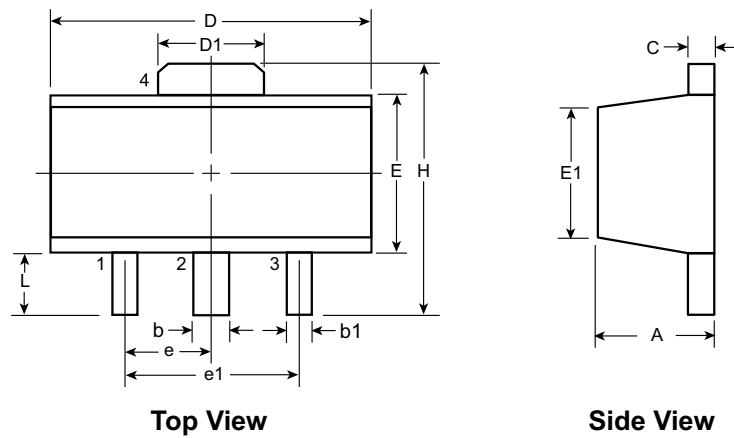
JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

## 3-Lead TO-243AA (SOT-89) Package Outline (N8)



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

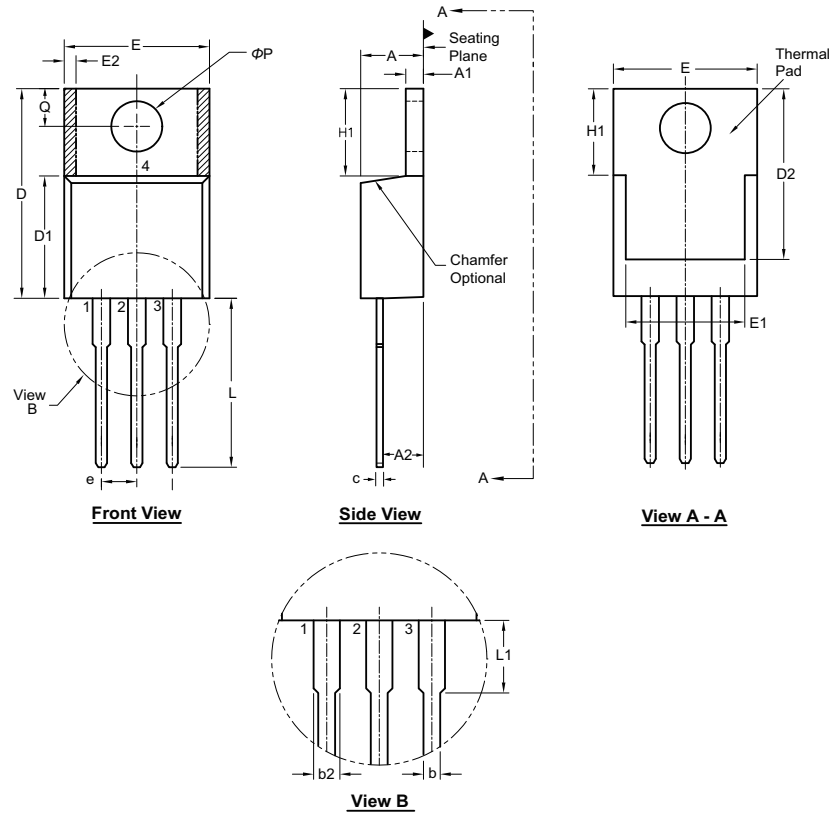
Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 <sup>†</sup>	1.50 BSC	3.00 BSC	3.94	0.73 <sup>†</sup>		
	NOM	-	-	-	-	-	-	-	-			-	-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20		

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

<sup>†</sup> This dimension differs from the JEDEC drawing

Drawings not to scale.

## 3-Lead TO-220 Package Outline (N5)



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

Symbol	A	A1	A2	b	b2	c	D	D1	D2	E	E1	E2	e	H1	L	L1	Q	ϕP		
Dimension (inches)	MIN	.140	.020	.080	.015	.045	.012 <sup>†</sup>	.560	.326 <sup>†</sup>	.474 <sup>†</sup>	.380	.270	0.20 <sup>*</sup>	.100 BSC	.230	.500	.200 <sup>*</sup>	.100	.139	
	NOM	-	-	-	.027	.057	-	-	-	-	-	-	-		-	-	-	-	-	-
	MAX	.190	.055	.120 <sup>†</sup>	.040	.070	.024	.650	.361 <sup>†</sup>	.507	.420	.350	.030		.270	.580	.250	.135	.161	

JEDEC Registration TO-220, Variation AB, Issue K, April 2002.

<sup>\*</sup> This dimension is not specified in the JEDEC drawing.

<sup>†</sup> This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

# DN2540

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision A (August 2022)

- Converted Doc# DSFP-DN2540 to Microchip DS20006717A
- Added some sections to comply with the standard Microchip format
- Changed the package marking format
- Removed the 3-lead TO-92 N3 P002, P005, P013, and P014 media types to align packaging specifications with the actual BQM
- Made minor text changes throughout the document

# DN2540

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	DN2540	=	N-Channel Depletion-Mode Vertical DMOS FET		
Packages:	N3	=	3-lead TO-92		
	N8	=	3-lead SOT-89		
	N5	=	3 lead TO-220		
Environmental:	G	=	Lead (Pb)-free/ROHS-compliant package		
Media Types:	(blank)	=	1000/Bag for an N3 package		
		=	200/Reel for an N8 package		
		=	50/Tube for an N5 package		
	P003	=	2000/Reel for an N3 package		

Examples:	
a) DN2540N3-G:	N-Channel Depletion-Mode, Vertical DMOS FET, 3-lead TO-92, 1000/Bag
b) DN2540N3-G-P003:	N-Channel Depletion-Mode, Vertical DMOS FET, 3-lead TO-92, 2000/Reel
c) DN2540N8-G:	N-Channel Depletion-Mode, Vertical DMOS FET, 3-lead SOT-89, 2000/Reel
d) DN2540N5-G:	N-Channel Depletion-Mode, Vertical DMOS FET, 3-lead TO-220, 50/Tube

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ISBN: 978-1-6683-1131-8



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